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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,631	07/01/2003	Shingo Ishihara	503.38289CC2	2368

20457 7590 08/09/2005

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/609,631	ISHIHARA ET AL.
	Examiner	Art Unit
	Joseph Nguyen	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/526,557.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the limitation "wherein the at least one gate electrode is above or beneath the semiconductor layer containing the gate insulating film" in claim 8 is not defined in the originally filed disclosure. Note that only "the at least one gate electrode is beneath the semiconductor layer contacting the gate insulating film" is defined as shown in figure 1(a) of the instant application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2, 4-6 and 8-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 6,593,977 B2 in view of Tanaka et al. (US 5,892,244).

Regarding claim 1, claims 1 and 3 of U.S. Patent No. 6,593,977 B2 disclose all the structure set forth in the claimed invention except said semiconductor layer being located so as to contact said gate insulating film only at regions acting as channel regions of the IC card apparatus. However, Tanaka et al. discloses in figure 3 said semiconductor layer 4 (col. 4, lines 38-39) being located so as to contact said gate insulating film 3 (col. 4, line 35) only at regions acting as channel regions of the IC card apparatus. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claims 1 and 3 of U.S. Patent No. 6,593,977 B2 by having said semiconductor layer being located so as to contact said gate insulating film only at regions acting as channel regions of the IC card apparatus to highly modulate a current flowing between the source and drain with a gate voltage (col. 3, lines 10-11, Tanaka et al.).

Regarding claim 2, claim 2 of U.S. Patent No. 6,593,977 B2 discloses the semiconductor layer is an organic semiconductor layer.

Regarding claim 4, claim 4 of U.S. Patent No. 6,593,977 B2 discloses the substrate is a plastic substrate.

Regarding claim 5, claim 5 of U.S. Patent No. 6,593,977 B2 discloses the plastic substrate is made of polymer material.

Regarding claim 6, claim 6 of U.S. Patent No. 6,593,977 B2 discloses the channel region has a size which is a same size as a gate electrode of the at least one gate electrode.

Regarding claim 11, claims 1 and 7 of U.S. Patent No. 6,593,977 B2 disclose all the structure set forth in the claimed invention except said semiconductor layer being located so as to contact said gate insulating film only at regions acting as channel regions of the IC card apparatus. However, Tanaka et al. discloses in figure 3 said semiconductor layer 4 (col. 4, lines 38-39) being located so as to contact said gate insulating film 3 (col. 4, line 35) only at regions acting as channel regions of the IC card apparatus. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claims 1 and 7 of U.S. Patent No. 6,593,977 B2 by having said semiconductor layer being located so as to contact said gate insulating film only at regions acting as channel regions of the IC card apparatus to highly modulate a current flowing between the source and drain with a gate voltage (col. 3, lines 10-11, Tanaka et al.).

Regarding claim 8, Tanaka et al. discloses in figure 3 the channel regions are between respective source and drain electrodes 5, 6 (col. 4, lines 34-36) of the at least one source electrode and the at least one drain electrode, wherein the respective source and drain electrodes contact opposite ends of the semiconductor layer 4 contacting the gate insulating film 3, and wherein the at least one gate electrode 2 (col. 4, line 22) is beneath the semiconductor layer contacting the gate insulating film.

Regarding claim 9, claim 6 of U.S. Patent No. 6,593,977 B2 discloses the channel region has a size which is a same size as a gate electrode of the at least one gate electrode.

Regarding claim 10, claim 2 of U.S. Patent No. 6,593,977 B2 discloses the semiconductor layer is an organic semiconductor layer.

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4-6 and 8-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
August 4, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER